# LH521002B

## CMOS 256K × 4 Static RAM

### FEATURES

- Fast Access Times: 17/20/25/35 ns
- JEDEC Standard Pinouts
- Low Power Standby when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- 2 V Data Retention (L Version)
- Packages:
  - 28-pin, 300-mil SOJ (Preliminary)
  - 28-pin, 400-mil SOJ

### FUNCTIONAL DESCRIPTION

The LH521002B is a high-speed 1M-bit static RAM organized as 256K × 4. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) reduces power to the chip when $\overline{E}$ is HIGH. Standby power drops to its lowest level when $\overline{E}$ is raised to within 0.2 V of $V_{CC}$.

Write cycles occur when both ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 18 address lines.

Read cycles occur when $\overline{E}$ is LOW and $\overline{W}$ is HIGH. A Read cycle will begin upon an address transition, on a falling edge of $\overline{E}$, or on a rising edge of $\overline{W}$.

The 'L' version will retain data down to a supply voltage of 2 V. A significantly lower current can be obtained ($I_{DR}$) under this Data Retention condition. CMOS Standby Current ($I_{SB2}$) is reduced on the 'L' version with respect to the standard version for those applications needing reduced power consumption.

High frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high frequency decoupling capacitors, are desirable. Series termination of the inputs should be considered when transmission line effects occur.

### PIN CONNECTIONS

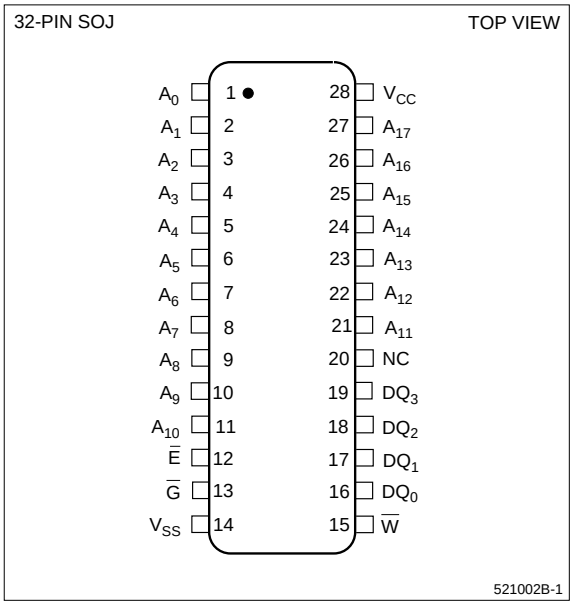



**Figure 1. Pin Connections for SOJ Package**

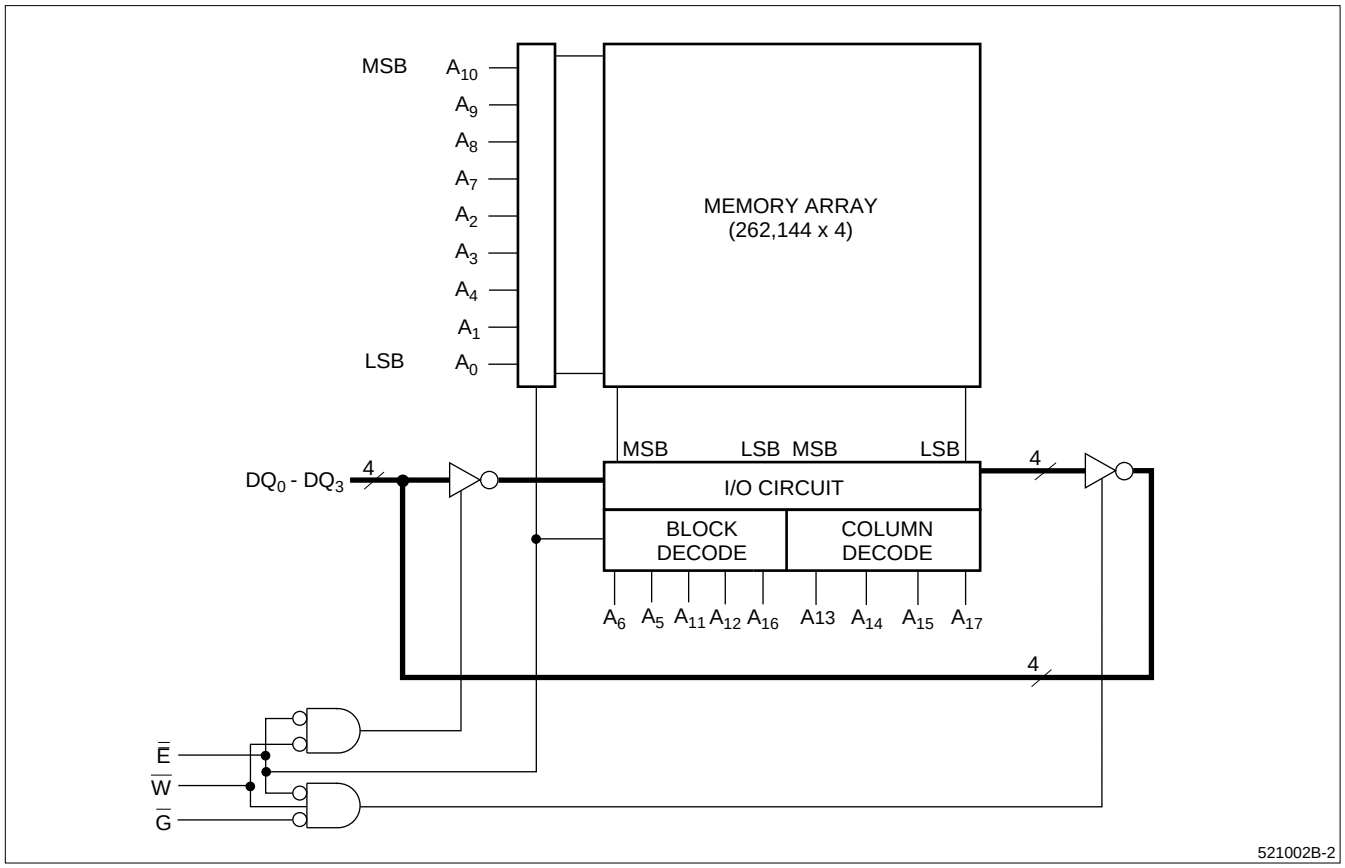



**Figure 2. LH521002B Block Diagram**

## TRUTH TABLE

| $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | MODE | DQ | $I_{CC}$ |
|---|---|---|---|---|---|
| H | X | X | Standby | High-Z | Standby |
| L | H | H | Selected | High-Z | Active |
| L | L | H | Read | Data Out | Active |
| L | X | L | Write | Data In | Active |

**NOTE:**
X = Don't Care, L = LOW, H = HIGH

## PIN DESCRIPTIONS

| PIN | DESCRIPTION |
|---|---|
| $A_0 – A_{17}$ | Address Inputs |
| $DQ_0 – DQ_3$ | Data Inputs/Outputs |
| $\overline{E}$ | Chip Enable |
| $\overline{W}$ | Write Enable |
| $\overline{G}$ | Output Enable |
| $V_{CC}$ | Positive Power Supply |
| $V_{SS}$ | Ground |

## ABSOLUTE MAXIMUM RATINGS [1]

| PARAMETER | RATING |
|---|---|
| $V_{CC}$ to $V_{SS}$ Potential | –0.5 V to 7 V |
| Input Voltage Range | –0.5 V to $V_{CC}$ + 0.5 V |
| DC Output Current [2] | ± 40 mA |
| Storage Temperature Range | –65°C to 150°C |
| Power Dissipation (Package Limit) | 1.0 W |

**NOTES:**

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

## OPERATING RANGES

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $T_A$ | Temperature, Ambient | 0 | | 70 | °C |
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{SS}$ | Supply Voltage | 0 | 0 | 0 | V |
| $V_{IL}$ | Logic '0' Input Voltage [1] | –0.5 | | 0.8 | V |
| $V_{IH}$ | Logic '1' Input Voltage | 2.2 | | $V_{CC}$ + 0.5 | V |

**NOTE:**

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

## DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CC1}$ | Operating Current [1] | $t_{CYCLE}$ = 17 ns | | 105 | 155 | mA |
| $I_{CC1}$ | Operating Current [1] | $t_{CYCLE}$ = 20 ns | | 95 | 140 | mA |
| $I_{CC1}$ | Operating Current [1] | $t_{CYCLE}$ = 25 ns | | 85 | 125 | mA |
| $I_{CC1}$ | Operating Current [1] | $t_{CYCLE}$ = 35 ns | | 85 | 125 | mA |
| $I_{SB1}$ | TTL Standby Current | $\overline{E} \geq V_{IH}$, $t_{CYC}$ = 17 ns, $I_{OUT}$ = 0 | | | 50 | mA |
| $I_{SB1}$ | TTL Standby Current | $\overline{E} \geq V_{IH}$, $t_{CYC}$ = 20 ns, $I_{OUT}$ = 0 | | | 45 | mA |
| $I_{SB1}$ | TTL Standby Current | $\overline{E} \geq V_{IH}$, $t_{CYC}$ = 25 ns, $I_{OUT}$ = 0 | | | 40 | mA |
| $I_{SB1}$ | TTL Standby Current | $\overline{E} \geq V_{IH}$, $t_{CYC}$ = 35 ns, $I_{OUT}$ = 0 | | | 35 | mA |
| $I_{SB2}$ | Standby Current | $\overline{E} \geq V_{CC}$ – 0.2 V, $t_{CYC}$ = 0, $I_{OUT}$ = 0 | | | 10 | mA |
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = 0 V to $V_{CC}$ | –2 | | 2 | µA |
| $I_{LO}$ | I/O Leakage Current | $V_{IN}$ = 0 V to $V_{CC}$ | –2 | | 2 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –4.0 mA | 2.4 | | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 8.0 mA | | | 0.4 | V |

**NOTE:**

1. $I_{CC}$ is dependent upon output loading and cycle rates. Specified values are with outputs open.

## AC TEST CONDITIONS

| PARAMETER | RATING |
|---|---|
| Input Pulse Levels | $V_{SS}$ to 3 V |
| Input Rise and Fall Times | 5 ns |
| Input and Output Timing Ref. Levels | 1.5 V |
| Output Load, Timing Tests | Figure 3 |

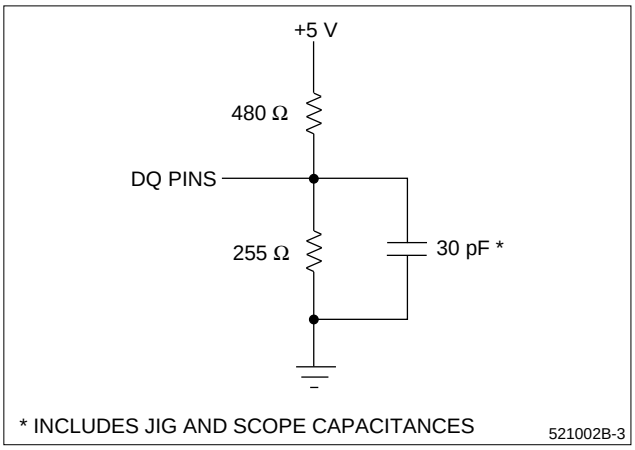



**Figure 3. Output Load Circuit**

## CAPACITANCE [1,2]

| PARAMETER | RATING |
|---|---|
| $C_{IN}$ (Input Capacitance) | 7 pF |
| $C_{DQ}$ (I/O Capacitance) | 8 pF |

**NOTE:**

1. Capacitances are maximum values at 25°C measured at 1 MHz with $V_{BIAS}$ = 0 V and $V_{CC}$ = 5.0 V.
2. Guaranteed but not tested.

## DATA RETENTION CHARACTERISTICS (For LH521002B-##L Version Only)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | 2 | | | V |
| $I_{SB2}$ | Standby Current | $\overline{E} \geq (V_{CC} - 0.2\ V)$<br>$V_{IN} \geq (V_{CC} - 0.2\ V)$ or $\leq 0.2$ V,<br>$t_{CYC} = 0$, $I_{OUT} = 0$ | | | 1.5 | mA |
| $I_{CCDR}$ | Data Retention Current | $V_{CC}$ = 3 V, $\overline{E} \geq (V_{CC} - 0.2\ V)$ | | | 250 | µA |
| $t_{CDRS}$ | Deselect to D.R. Time | | 0 | | | ns |
| $t_R$ | Operation Recovery Time | | $t_{RC}$ | | | ns |

## DATA RETENTION TIMING

For data retention mode, $\overline{E} \geq V_{CC} - 0.2$ V. All other inputs must meet: $V_{CC} - 0.2\ V \leq V_{IN} \leq 0.2$ V.

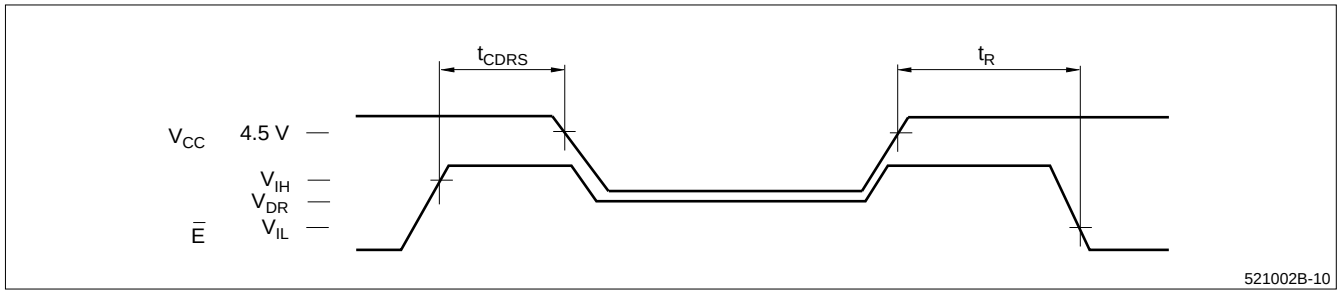



**Figure 4. Data Retention Timing**

## AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

| SYMBOL | DESCRIPTION | –17 | | –20 | | –25 | | –35 | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| **READ CYCLE** | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Timing | 17 | | 20 | | 25 | | 35 | | ns |
| $t_{AA}$ | Address Access Time | | 17 | | 20 | | 25 | | 35 | ns |
| $t_{OH}$ | Output Hold from Address Change | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{EA}$ | $\overline{E}$ Low to Valid Data | | 17 | | 20 | | 25 | | 35 | ns |
| $t_{ELZ}$ | $\overline{E}$ Low to Output Active [2,3] | 5 | | 5 | | 5 | | 5 | | ns |
| $t_{EHZ}$ | $\overline{E}$ High to Output High-Z [2,3] | | 8 | | 8 | | 10 | | 15 | ns |
| $t_{GA}$ | $\overline{G}$ Low to Valid Data | | 7 | | 7 | | 8 | | 12 | ns |
| $t_{GLZ}$ | $\overline{G}$ Low to Output Active [2,3] | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{GHZ}$ | $\overline{G}$ High to Output High-Z [2,3] | | 6 | | 6 | | 10 | | 20 | ns |
| $t_{PU}$ | $\overline{E}$ Low to Power Up Time [3] | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PD}$ | $\overline{E}$ High to Power Down Time [3] | | 17 | | 20 | | 25 | | 35 | ns |
| **WRITE CYCLE** | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 17 | | 20 | | 25 | | 35 | | ns |
| $t_{EW}$ | $\overline{E}$ Low to End of Write | 12 | | 12 | | 15 | | 20 | | ns |
| $t_{AW}$ | Address Valid to End of Write | 12 | | 12 | | 15 | | 20 | | ns |
| $t_{AS}$ | Address Setup | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{AH}$ | Address Hold From End of Write | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WP}$ | $\overline{W}$ Pulse Width | 12 | | 12 | | 15 | | 20 | | ns |
| $t_{DW}$ | Input Data Setup Time | 9 | | 9 | | 10 | | 12 | | ns |
| $t_{DH}$ | Input Data Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WHZ}$ | $\overline{W}$ Low to Output High-Z [2,3] | 0 | 7 | 0 | 8 | 0 | 10 | 0 | 15 | ns |
| $t_{WLZ}$ | $\overline{W}$ High to Output Active [2,3] | 3 | | 3 | | 3 | | 3 | | ns |

**NOTES:**

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±200 mV transition from steady state levels into the test load. $C_{Load}$ = 5 pF.
3. Guaranteed but not tested.

## TIMING DIAGRAMS – READ CYCLE

### Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of DQ implies that data lines are in the Low-Z state and the data may not be valid.

### Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid while $\overline{E}$ goes LOW. Data Out is not specified to be valid until $t_{EA}$, but may become valid as soon as $t_{ELZ}$. Outputs will transition from High-Z to Valid Data Out. Data Out is valid after both $t_{EA}$ and $t_{GA}$ are met.

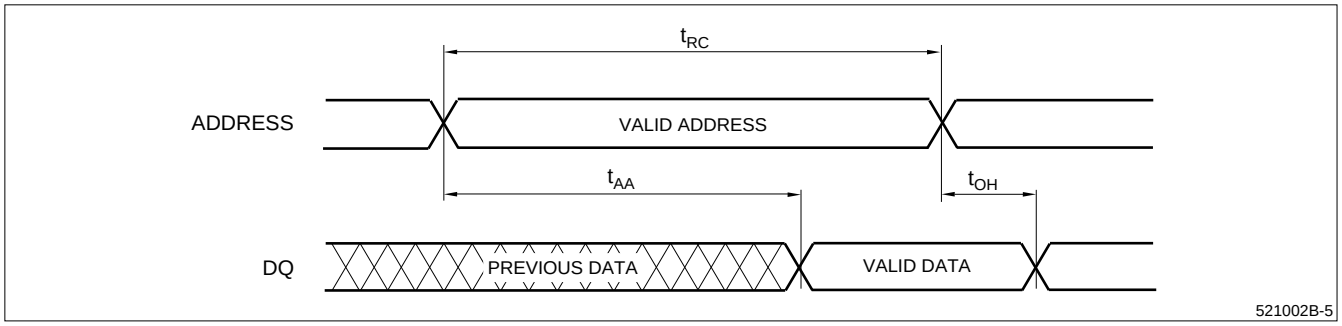



**Figure 5. Read Cycle No. 1**

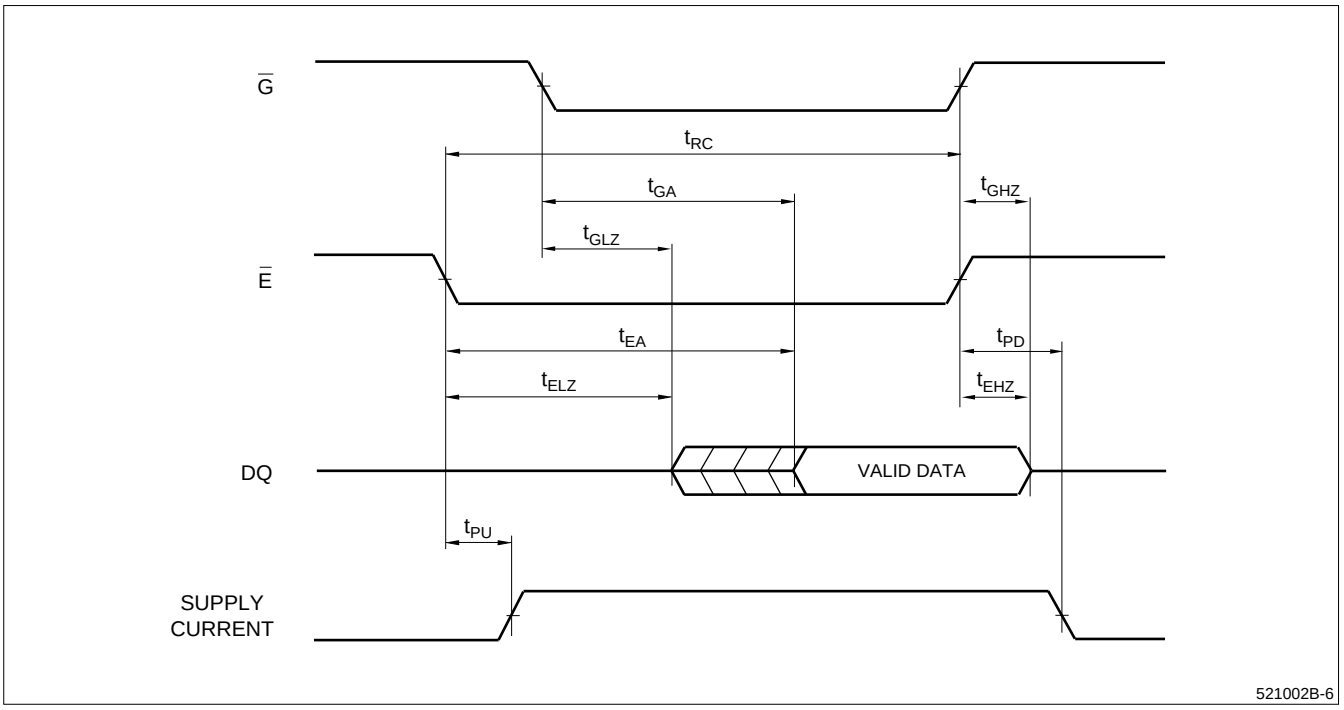



**Figure 6. Read Cycle No. 2**

## TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. $\overline{E}$ or $\overline{W}$ must be HIGH during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise.

### Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ and $\overline{G}$ are LOW. Using only $\overline{W}$ to control Write cycles may not offer the best device performance, since both $t_{WHZ}$ and $t_{DW}$ timing specifications must be met.

### Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

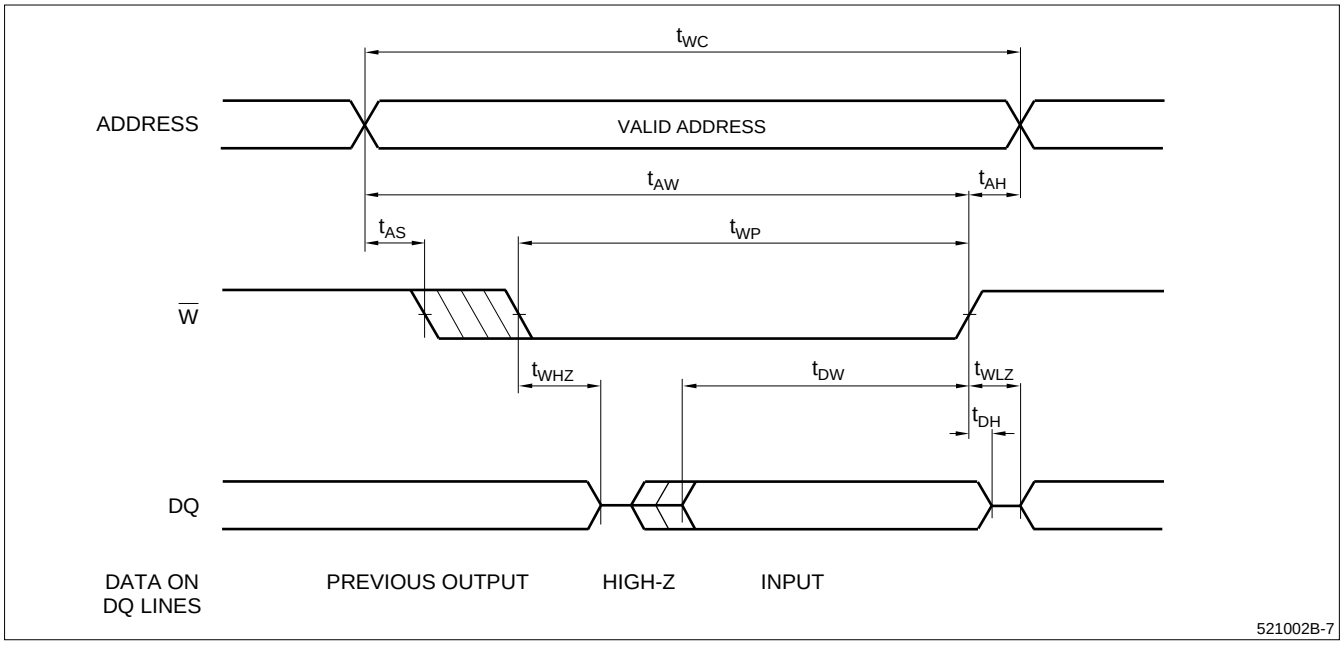



**Figure 7. Write Cycle No. 1**

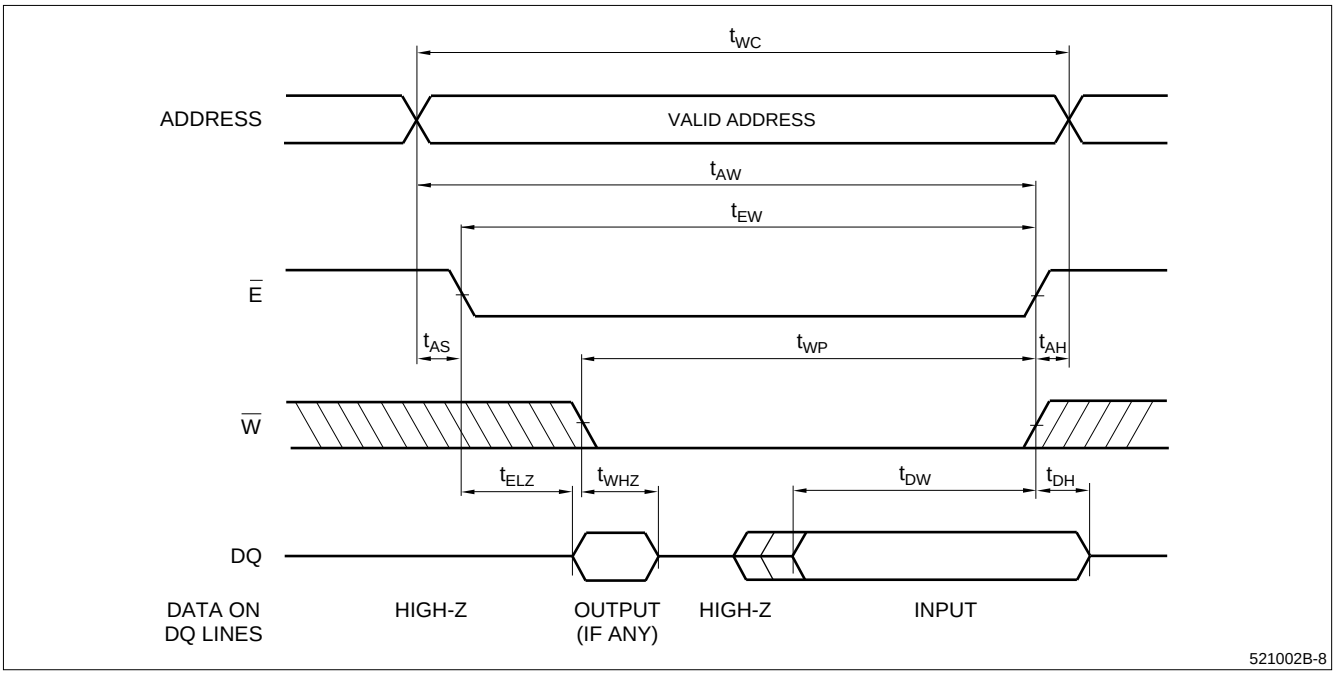
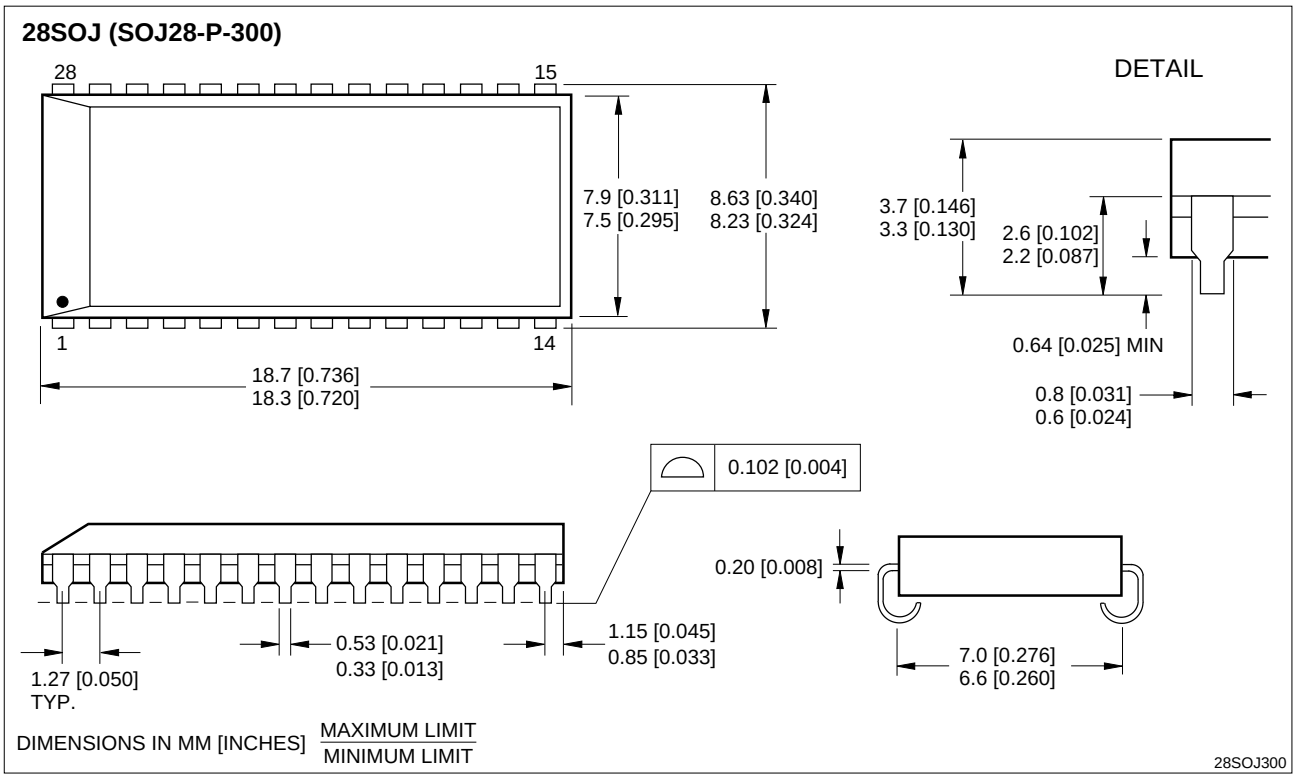
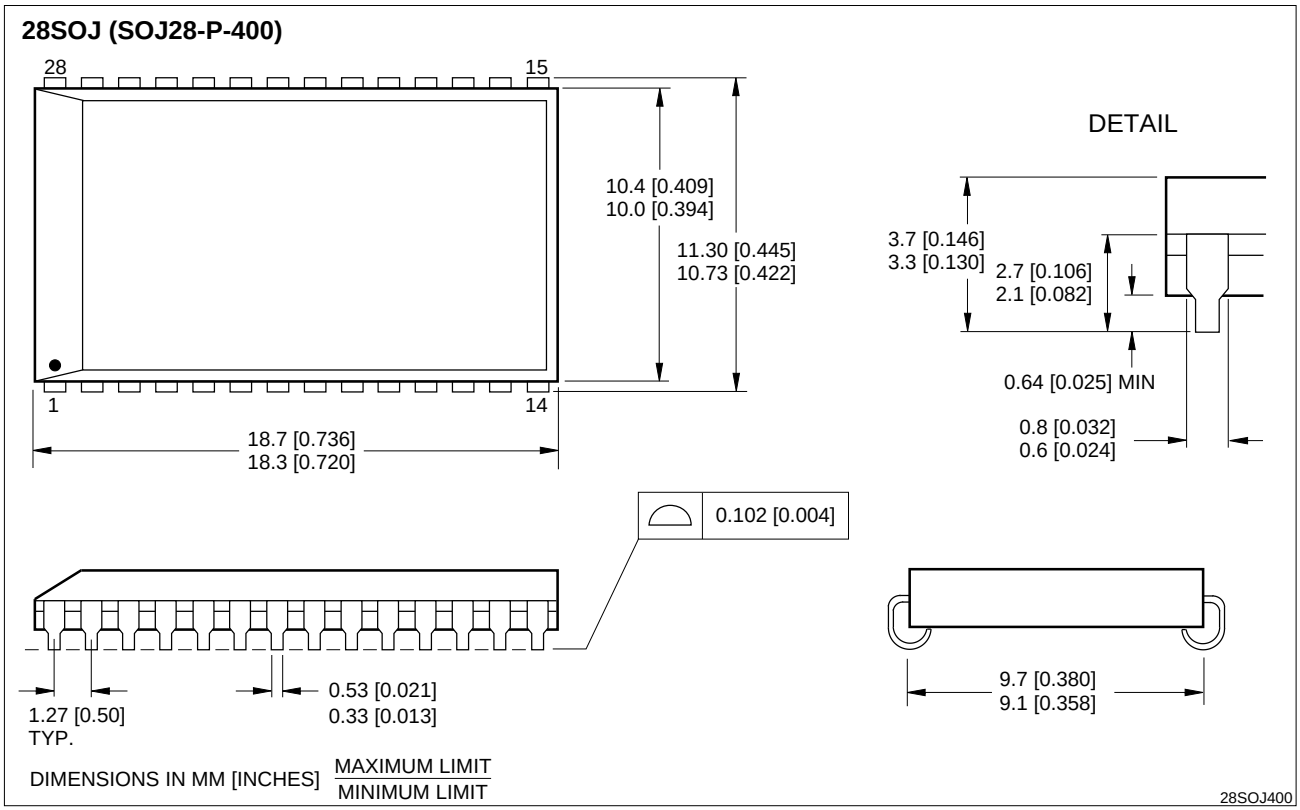



**Figure 8. Write Cycle No. 2**

## PACKAGE DIAGRAMS

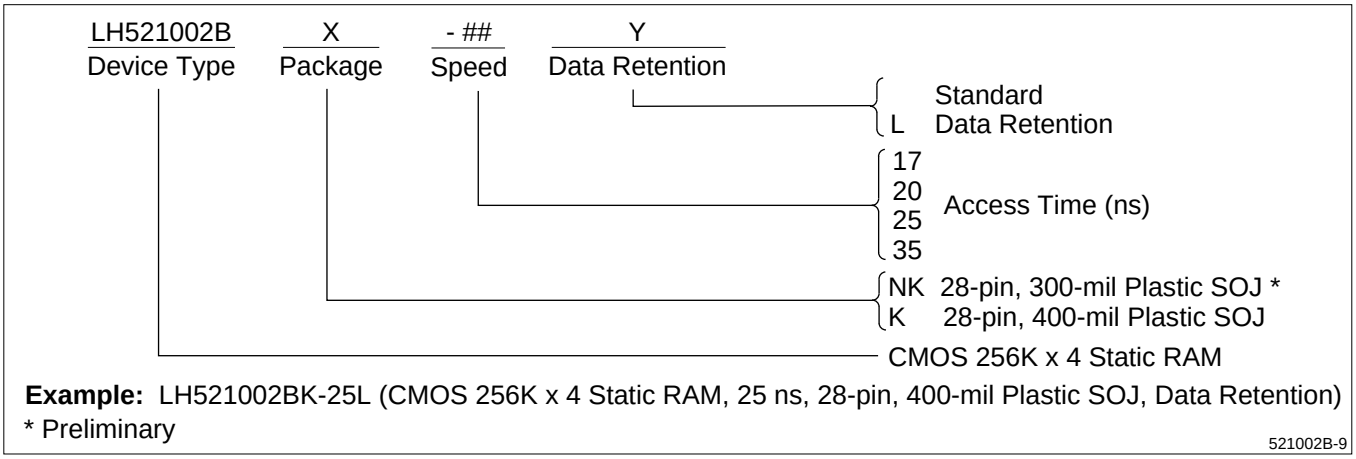



**28-pin, 300-mil SOJ (Preliminary)**




**28-pin, 400-mil SOJ**

## ORDERING INFORMATION




**Example:** LH521002BK-25L (CMOS 256K x 4 Static RAM, 25 ns, 28-pin, 400-mil Plastic SOJ, Data Retention)

* Preliminary

521002B-9